WHAT IS CLAIMED IS:

1. A semiconductor memory device comprising:

a storage capacity element portion comprising a plurality of capacitors that constitute memory cells and have the same shape,

wherein an interlayer insulating film has a plurality of trenches in which storage nodes are buried separately and a capacitor insulating film and a plate electrode are buried in common so as to form the capacitors, and

any capacitor is arranged so that only a part of a side face of one trench is opposite to that of the other.

2. The semiconductor memory device according to claim 1, wherein a relative dielectric constant of the interlayer insulating film is smaller than that of a silicon oxide film.

3. A semiconductor memory device comprising:

a storage capacity element portion comprising a plurality of capacitors that constitute memory cells and have the same shape,

wherein an interlayer insulating film has a plurality of trenches in which storage nodes are buried separately and a capacitor insulating film and a plate electrode are buried in common so as to form the capacitors, and

any capacitor is arranged so that a side face of one trench is opposite completely to that of the other, and has a shape in which a distance between opposing side faces is larger at central portions of the respective trenches.

4. The semiconductor memory device according to claim 3, wherein a relative dielectric constant of the interlayer insulating film is smaller than that of a silicon oxide film.

5. A semiconductor memory device comprising:

a storage capacity element portion comprising a plurality of capacitors that constitute memory cells and have the same shape,

wherein an interlayer insulating film has a plurality of trenches in which storage nodes are buried separately and a capacitor insulating film and a plate electrode are buried in common so as to form the capacitors, and

a concavity is provided between the adjacent capacitors and the plate electrode is buried in the concavity.

6. The semiconductor memory device according to claim 5, wherein a relative dielectric constant of the interlayer insulating film is smaller than that of a silicon oxide film.

7. A method for manufacturing a semiconductor memory device comprising:

depositing an interlayer insulating film on a semiconductor substrate provided with contact plugs;

pattering a mask pattern on the interlayer insulating film, the mask pattern having a layout in which a plurality of hole patterns having the same shape are arranged so that the adjacent hole patterns are only partially opposite to each other;

forming holes for storage nodes in the interlayer insulating film by etching with the mask pattern;

forming the storage nodes in the holes so as to be connected electrically to the contact plugs;

forming a capacitor insulating film on the storage nodes; and

forming a plate electrode on the capacitor insulating film.

8. The method according to claim 7, wherein a relative dielectric constant of the interlayer insulating film is smaller than that of a silicon oxide film.

9. A method for manufacturing a semiconductor memory device comprising:

depositing an interlayer insulating film on a semiconductor substrate provided with contact plugs;

pattering a mask pattern on the interlayer insulating film, the mask pattern having a layout in which a plurality of hole patterns having the same shape are arranged so that the adjacent hole patterns are opposite to each other, and a distance between the opposing hole patterns is larger at central portions of the respective hole patterns;

forming holes for storage nodes in the interlayer insulating film by etching with the mask pattern;

forming the storage nodes in the holes so as to be connected electrically to the contact plugs;

forming a capacitor insulating film on the storage nodes; and
forming a plate electrode on the capacitor insulating film.

10. The method according to claim 9, wherein a relative dielectric constant of the interlayer insulating film is smaller than that of a silicon oxide film.

11. A method for manufacturing a semiconductor memory device comprising:

depositing an interlayer insulating film on a semiconductor substrate provided with contact plugs;

patterning a mask pattern on the interlayer insulating film, the mask pattern having a layout in which a plurality of hole patterns having the same shape are arranged so that the adjacent hole patterns are opposite to each other;

forming holes for storage nodes in the interlayer insulating film by etching with the mask pattern;

forming the storage nodes in the holes so as to be connected electrically to the contact plugs;

forming a capacitor insulating film on the storage nodes; and

forming a plate electrode on the capacitor insulating film,

wherein the mask pattern is patterned with a pitch of the hole patterns that makes a distance between opposing central portions of the adjacent storage nodes larger than a distance between opposing corners thereof due to proximity effect during formation of the storage nodes.

12. The method according to claim 11, wherein the pitch is smaller than 0.55 μm.

13. The method according to claim 11, wherein a relative dielectric constant of the interlayer insulating film is smaller than that of a silicon oxide film.

14. A method for manufacturing a semiconductor memory device comprising:

depositing an interlayer insulating film on a semiconductor substrate provided with contact plugs;

patterning a mask pattern on the interlayer insulating film, the mask pattern having a layout in which a plurality of hole patterns having the same shape are arranged so that the adjacent hole patterns are opposite to each other;

forming holes for storage nodes in the interlayer insulating film by etching with the mask pattern;

forming the storage nodes in the holes so as to be connected electrically to the contact plugs;

etching an upper potion of the interlayer insulating film between the storage nodes;

forming a capacitor insulating film on the storage nodes; and

forming a plate electrode on the capacitor insulating film.

15. The method according to claim 14, wherein a relative dielectric constant of the interlayer insulating film is smaller than that of a silicon oxide film.

ABSTRACT OF THE DISCLOSURE

A DRAM is provided that can reduce the parasitic capacitance between trench-type stacked cell capacitors in a memory cell region and suppress malfunction caused by noise. The trench-type stacked cell includes a number of capacitors having the same shape. The capacitors are formed in such a manner that storage nodes, a capacitor insulating film, and a plate electrode are buried in each of a plurality of trenches of an interlayer insulating film. The cell layout can be as follows: the capacitors are arranged so that only a part of a side face of one trench is opposite to that of the other; the capacitors are arranged so that the side face of one trench is opposite completely to that of the other and the distance between the opposing side faces is larger at the central portions of the respective trenches; or the cell is arranged so that the plate electrode is buried in a concavity between the cell capacitors.